WHAT IS CLAIMED IS:

1. A CMOS sensor circuit comprising:
a photodiode;
a reset transistor resetting said photodiode to an initial voltage; and
a voltage control circuit controlling a gate potential of said reset transistor to a potential other than power source potentials.

2. A CMOS sensor circuit comprising:
a photodiode;
a reset transistor resetting said photodiode to an initial voltage; and
a voltage control circuit keeping a gate potential of said reset transistor from completely becoming off.

3. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:
an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and
a transistor inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a

blooming.

4. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

5. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor connected to a drain of said N-channel MOS transistor so as to control a blooming.

6. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said

reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

a transistor connected to a drain of said N-channel MOS transistor so as to control a blooming.

7. The CMOS sensor circuit as claimed in claim 3, further comprising a plurality of serially connected transistors inserted between said drain of said first P-channel MOS transistor and said drain of said N-channel MOS transistor so as to control the blooming.

8. The CMOS sensor circuit as claimed in claim 4, further comprising a plurality of serially connected transistors inserted between said drain of said first P-channel MOS transistor and said drain of said N-channel MOS transistor so as to control the blooming.

9. The CMOS sensor circuit as claimed in claim 5, further comprising a plurality of serially connected transistors connected to said drain of said N-channel MOS transistor so as to control the blooming.

10. The CMOS sensor circuit as claimed in claim 6, further comprising a plurality of serially connected transistors connected to said drain of said N-channel MOS transistor so as to control the blooming.

11. The CMOS sensor circuit as claimed in claim 3, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor.

12. The CMOS sensor circuit as claimed in claim 4, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor.

13. The CMOS sensor circuit as claimed in claim 3, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

14. The CMOS sensor circuit as claimed in claim 4, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS

transistor, and includes a gate and a drain connected to each other.

15. The CMOS sensor circuit as claimed in claim 5, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

16. The CMOS sensor circuit as claimed in claim 6, wherein said transistor is one of a P-channel MOS transistor and an N-channel MOS transistor, and includes a gate and a drain connected to each other.

17. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

18. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element inserted between a drain of said first P-channel MOS transistor and a drain of said N-channel MOS transistor so as to control a blooming.

19. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode element connected to a drain of said N-channel MOS transistor so as to control a blooming.

20. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises:

an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor and an N-channel MOS transistor; and

one of a resistance element and a diode

element connected to a drain of said N-channel MOS transistor so as to control a blooming.

21. The CMOS sensor circuit as claimed in claim 17, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

22. The CMOS sensor circuit as claimed in claim 18, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

23. The CMOS sensor circuit as claimed in claim 19, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

24. The CMOS sensor circuit as claimed in

claim 20, wherein said resistance element and said diode element are replaced by a plurality of serially connected resistance elements and a plurality of serially connected diode elements, respectively.

25. The CMOS sensor circuit as claimed in claim 1, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal, an N-channel MOS transistor having a gate supplied with a second signal, and a transistor used for controlling a blooming.

26. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises an inverter circuit driving a gate of said reset transistor, the inverter circuit including a first P-channel MOS transistor having a gate supplied with a first signal, an N-channel MOS transistor having a gate supplied with a second signal, and a transistor used for controlling a blooming.

27. The CMOS sensor circuit as claimed in claim 25, further comprising a delay circuit

producing said first signal by delaying said second signal.

28. The CMOS sensor circuit as claimed in claim 26, further comprising a delay circuit producing said first signal by delaying said second signal.

29. The CMOS sensor circuit as claimed in claim 27, said delay circuit is formed by an even number of inverters.

30. The CMOS sensor circuit as claimed in claim 28, said delay circuit is formed by an even number of inverters.

31. The CMOS sensor circuit as claimed in claim 3, an arbitrary bias voltage is applied to said transistor.

32. The CMOS sensor circuit as claimed in claim 4, an arbitrary bias voltage is applied to

said transistor.

33. The CMOS sensor circuit as claimed in claim 5, an arbitrary bias voltage is applied to said transistor.

34. The CMOS sensor circuit as claimed in claim 6, an arbitrary bias voltage is applied to said transistor.

35. The CMOS sensor circuit as claimed in claim 2, wherein said voltage control circuit comprises an output node connected to a gate of said reset transistor, and a constant current source added to said output node.

36. The CMOS sensor circuit as claimed in claim 35, wherein said constant current source is formed by a second P-channel MOS transistor having a bias voltage applied to a gate voltage thereof.